WHAT IS CLAIMED IS:

1. A random access memory comprising:

memory banks; and

precharge timers configured to provide precharge signals to the memory banks, wherein each of the precharge timers corresponds to one of the memory banks and each of the precharge timers is configured to provide one of the precharge signals to the corresponding one of the memory banks in normal mode and in test mode.

2. The random access memory of claim 1, comprising a burst control circuit configured to provide a burst end signal that indicates the end of a first burst from a first one of the memory banks.

3. The random access memory of claim 2, comprising a delay circuit configured to receive the burst end signal and provide a delayed burst end signal at the end of a second burst from a second one of the memory banks in test mode.

4. The random access memory of claim 3, comprising a precharge timer enable circuit configured to provide a precharge timer enable signal that indicates the beginning of the first burst from the first one of the memory banks.

5. The random access memory of claim 4, wherein the delay circuit is configured to receive the precharge timer enable signal and provide a delayed precharge timer enable signal that indicates the beginning of the second burst from the second one of the memory banks in test mode.

6. The random access memory of claim 5, wherein a first one of the precharge timers is configured to provide a first one of the precharge signals in response to the burst end signal after receiving the precharge timer enable signal

and a second one of the precharge timers is configured to provide a second one of the precharge signals in response to the delayed burst end signal after receiving the delayed precharge timer enable signal.

7. The random access memory of claim 3, wherein the delay circuit comprises a shift register.

8. The random access memory of claim 1, comprising a precharge timer enable circuit configured to provide a precharge timer enable signal to indicate the beginning of a first burst from a first one of the memory banks.

9. The random access memory of claim 8, comprising a delay circuit configured to receive the precharge timer enable signal and provide a delayed precharge timer enable signal that indicates the beginning of a second burst from a second one of the memory banks in test mode.

10. The random access memory of claim 1, comprising a burst control circuit configured to provide a burst end signal that indicates the end of each burst from each of the memory banks in normal mode.

11. The random access memory of claim 10, wherein each precharge timer is configured to provide the one of the precharge signals to the corresponding one of the memory banks in response to receiving a precharge timer enable signal for the corresponding one of the memory banks and the burst end signal.

12. The random access memory of claim 1, comprising a precharge timer enable circuit configured to provide precharge timer enable signals to indicate the beginning of each burst from each of the memory banks in normal mode.

13. The random access memory of claim 12, wherein each precharge timer is configured to provide the one of the precharge signals to the corresponding one

of the memory banks in response to receiving one of the precharge timer enable signals for the corresponding one of the memory banks and a burst end signal.

14. The random access memory of claim 1, comprising a multiplexer configured to supply a burst end signal and a precharge timer enable signal to one of the precharge timers in normal mode and a delayed burst end signal and a delayed precharge timer enable signal to the one of the precharge timers in test mode.

15. The random access memory of claim 1, wherein each of the precharge timers is configured to delay and synchronize with a clock signal the one of the precharge signals provided to the corresponding one of the memory banks.

16. The random access memory of claim 1, wherein each of the precharge timers is configured to asynchronously provide the one of the precharge signals to the corresponding one of the memory banks.

17. A memory control circuit comprising:

an enable circuit configured to provide a first enable signal that indicates the beginning of a first burst from a first memory bank;

a burst control circuit configured to provide a first burst end signal that indicates the end of the first burst from the first memory bank;

a delay circuit configured to delay the first enable signal and the first burst end signal in test mode; and

a precharge timer configured to provide a first precharge signal to a second memory bank in response to receiving the delayed first burst end signal and the delayed first enable signal.

18. The memory control circuit of claim 17, wherein:

the enable circuit is configured to provide a second enable signal that indicates the beginning of a second burst from the second memory bank in normal mode;

the burst control circuit is configured to provide a second burst end signal that indicates the end of the second burst from the second memory bank in normal mode; and

the precharge timer is configured to provide a second precharge signal to the second memory bank in response to receiving the second burst end signal and the second enable signal in normal mode.

19. The memory control circuit of claim 17, wherein the precharge timer is configured to provide the first precharge signal one clock cycle after receiving the delayed first burst end signal.

20. The memory control circuit of claim 17, wherein the precharge timer is configured to provide the first precharge signal asynchronously after receiving the delayed first burst end signal.

21. The memory control circuit of claim 17, wherein the delay circuit comprises a shift register.

22. The memory control circuit of claim 17, comprising a multiplexer configured to receive the delayed first burst end signal and the delayed first enable signal and provide the delayed first burst end signal and the delayed first enable signal to the precharge timer in the test mode.

23. A random access memory comprising:

means for supplying a signal that indicates the end of a data burst;

means for delaying the signal;

means for synchronizing the delayed signal with a clock signal;

means for supplying a first precharge signal to a first memory bank in response to the signal; and

means for supplying a second precharge signal to a second memory bank in response to the delayed and synchronized signal.

24. The random access memory of claim 23, wherein the means for delaying the signal and the means for synchronizing the delayed signal comprises a shift register.

25. The random access memory of claim 23, comprising:

means for selecting the delayed and synchronized signal in test mode.

26. The random access memory of claim 23, wherein the means for selecting the delayed and synchronized signal in test mode comprises a multiplexer.

27. A method of automatically precharging in a random access memory, comprising

supplying a first signal that indicates the end of a first data burst;

supplying a second signal in normal mode that indicates the end of a second data burst;

delaying the first signal in test mode;

selecting the second signal in normal mode and the delayed first signal in test mode;

supplying a precharge signal from a precharge timer in response to the selected signal.

28. The method of claim 27, comprising:

supplying a first enable signal;

delaying the first enable signal in test mode;

supplying the delayed first enable signal to the precharge timer in test mode.

29. The method of claim 28, comprising:

supplying a second enable signal in normal mode; and

supplying the second enable signal to the precharge timer in normal mode.

30. The method of claim 27, wherein supplying the precharge signal comprises:

delaying the precharge signal; and

synchronizing the precharge signal to a clock signal.

31. The method of claim 27, wherein supplying the precharge signal comprises:

supplying the precharge signal asynchronously in response to the selected signal.

32. The method of claim 27, comprising:

supplying the first data burst and the second data burst in sequential order in normal mode; and

interleaving the first data burst and the second data burst in test mode.